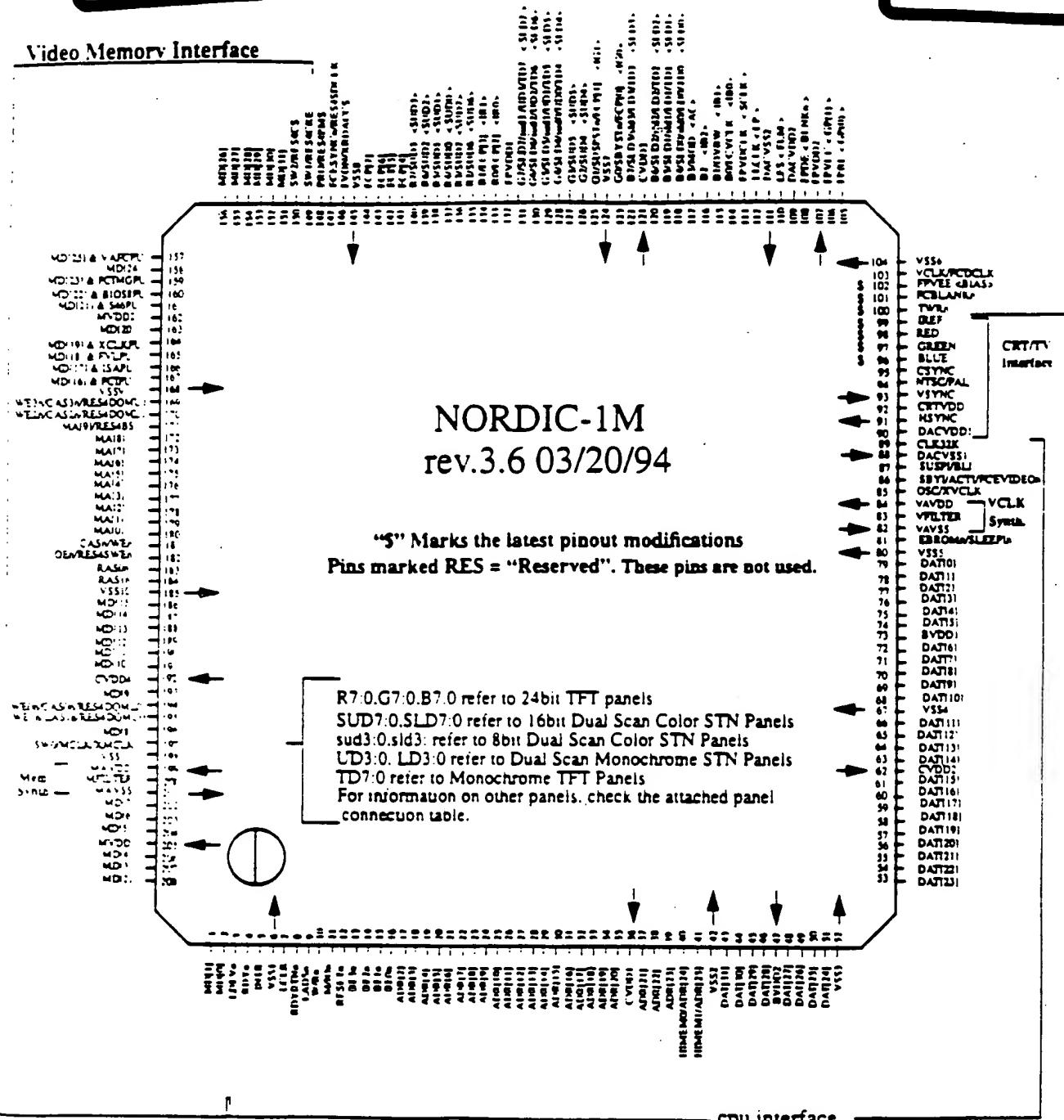




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EXHIBIT
EX-463C

Video Memory Interface



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DELTA LIST OVER PREVIOUS PINOUT RELEASED ON :

08/26/93:

- no POUT on SW2/POUT
- XVCLK moved from SW1/VCLK/XVCLK to OSC/XVCLK. This way SW1/VCLK/XVCLK became SW1/VCLK.

09/06/93

- All panel pins whose names were not starting with the color panel name were changed such that the names start now with the color panel pin (R7, G7, B7 and so on). So it was only a pin name change.

09/12/93 rev. 1.0 and 1.1

- 1. Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2. Reduced the number of CPU Address Pins: ADR[24..27] went-away. Use HIMEM to place the chip outside 16MB of memory for linear addressing.

3. Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI.
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector).

ADR[27..24] become VAFC pins. and R[7..4], G[7..6], CLK32K, SUSPI/BLI, SBY1/ACT1 get a configuration for VAFC -> total 14 pins.

SW0/VCLK will be used as VAFC DCLK. losing SW0 pin as panel type when VAFCPU is used.

In PCI bus, no ADR pin will be shared with VAFC

ASW0PL will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. SW0PL will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme. The chip will draw more power in suspend with VAFC.

5. Moved SW2, SW1/MCLK/XMCLK, the two RESERVED pins and TRWn on MVDD to prepare for SDRAM pin combination option in the next Nordic that supports SDRAMs. It looks that we need only 3 more memory pins to support SDRAM-s so TRWn will not be used. It was moved so it is on the right VDD bus if needed.

6. Moved CVDD3, VSS3, VCLK Synth. H/VSYNC, EROMn, SW0 per Thomas Hung's request to fit the floor plan.

09/21/93

1. Added ALXS1 on D/Cn as an option to be used with CS4231S as CS.

2. Added ALXS2 on EROMn/VADRn as an option to be used for Sound Synthesizer Chip Select.

3. Rearranged 5428 FC pins due to a previous error : R5 and R4 should not be used with FC.

- FCP[1..0] are shared with G7 and G6.

- SW2 and the two pins reserved for SDRAM were moved in between Video Memory pins and Panel pins and one of them is used as FCESYNCn.

- OVRW is shared with CLK32K. FCBLANKn is shared with SUSPI and FCEVIDEn is on SBY1.

4. Renamed the External Clock PU XCLKPU instead of XMCPU.

10/11/93 rev. 1.3

1. Moved some external pull-ups.

2. Added alternate pin functions on panel pins, as well as actual schematic name for engineering

10/27/93

1. Added TV-OUT (called also NTSC-OUT) pins on the panel pins

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10/28/93 rev. 1.5 Modifications

1. Added TVG on EBROMn/AUXS2 and took out VADR as an option on this pin.
2. Put back FCESYNCn on RES4SDCLK as an option (deleted by mistake).

11/11/93 rev. 2.0 Modifications

1. Reset became RESETn, active L to correspond with the defined reset signal for VESA VL and PCI.
2. TFT Panels Data Pins R7:R0, G7:G0, B7:B0 changed and all pins got rotated to get them ordered from right to left. Due to this change now Rj=TVRj, Gj=TVGj and Bj=TVBj.

01/06/94 rev. 3.0 Modifications

1. Update Panel Data Pins based on Robin's Table.
2. Move MOD pin on a Panel Data Pin used in 18bit TFT.
3. Move OVRW on a 24bit Panel Data Pin.
4. Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV... were removed. As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now.
5. Removed WavePort pins, including AUDVDD: total 7 pins freed.
6. AUX2 and TVG muxed on EBROMn are no longer needed either.
7. Added one more CPU address pin: instead of HMEM. Nordic has now HMEM0 and HMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the process of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin.
8. Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers.
9. EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on-chip BIOS support, AD720 power on cannot be directly controlled by Nordic.
10. Added pins for Analog TV Encoder support - AD720 and MC1377:
 - a CSYNC = Composite Sync signal
 - b. NTSC/PAL = 1 -> NTSC, 0-> PAL (for AD720, but it is TV Encoder Dependent)
 - c. EBROMn/TVON (see #8)
11. De-multiplexed some of the pins previously multiplexed:
 - a. Pin 168 TWRn/RES4PMS is now RES4PMS, a pin reserved for synchronous DRAM support.
 - b. SUSPI/BLI/FCBLANKn is now SL'SPI/BLI, not affected by the Feature Connector Enable Configuration
 - c. As a consequence of b, pin 97 is FCBLANKn (not muxed with anything). Please note that FCEVIDEOn is still muxed with SBYn/ACTn as before, as Standby Input and Keyboard Activity are less important functions in a system.
 - d. SW0 is no longer muxed on VCLK/FCDCLK. So VLK/FCDCLK is a pin but it is moved to pin 103 in the PVDD area, to be consistent with FC power supply.
12. SW1, muxed on MCLK/XMCLK (pin 197) became SW0. This is just a name change to have the switches placed in a more consistent manner.

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13. SW1 is now muxed with a reserved pin: RES4CKE, pin 148, which before was totally reserved. The idea here is to go for pwpd with SDRAM-s for SW2 and SW1, while keeping SW0 on MCLK even with SDRAM-s.
14. Pin 147 is Reserved. It is actually one of the WavePort pins, but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility. To achieve this, the pins on its right were moved to the right by one FPVEE <BLAS> moved down to pin 98 (it was 105).
15. TRWn is now by itself on pin 96, on FPVDD.
16. The names of all flat panel data pins reflect the panel type table attached to this document.

01/13/94 rev. 3.1 Modifications

1. On EBROMn/TVON -> EBROMn/SLEEPIn with SLEEPIn an input which if L puts Nordic to sleep (as 3C3[0] and 46E8(3)).
2. TVON is now on RES, but TVON/RES is pin 146 and FCESYNCn/RES4SDCLK is pin 147.

01/22/94 rev. 3.2 Modifications

1. Pin 148, RES4PMS which was a pin reserved for synchronous DRAM-s, got a function: it is now a programmable output PRO and it is on FPVDD instead of MVDD. The intention is to optionally use this pin to control a switch between 5V and 3.3V, in which case a H level of 5V is desirable. My primary choice for this function is actually NTSC/PAL pin which is on CRTVDD, but if the TV-OUT option is used in a system and a switch between 5 and 3.3V is provided, PRO may be used.

02/05/94 rev. 3.3 Modifications

1. Updated panel interface table with correct Nordic pin numbers. The pins shifted a bit in the last rev, but the panel interface table was not updated.

02/28/94 rev. 3.4 Modifications

1. TVON pin can be configured as XRDACCS "External RAMDAC Chip Select", H if access to 3C6:3c9 but not for 3C7 IORD, otherwise L. This way Nordic can support External RAMDAC through the feature connector and generate a chip select for it, so that with minimal external logic a RAMDAC IORD and IOWR can be generated. In previous versions, EBROMn could be used as External RAMDAC Chip Select only in ISA, because in any other bus configuration EBROMn became SLEEPIn input. SR25[6] configures TVON pin as XRDACCS. At POST this bit is TVON but it is reset to L, so in both TV-OUT systems and External RAMDAC systems, this bit will have no effect until we need it to (in both cases the pin is active H).

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2. TWRn pin name was wrong (was TRWn).

03/06/94 rev. 3.5 Modifications

1. PCINBPL (PCI NO_Burst Pull-Up) was replaced by PCIMGPU (PCI Memory_Grant Pull-Up) on MD[23]. GRE[4] enables PCI Burst and the default is disabled. A pull-up on PCIMGPU extends Mem_Gnt value from 250nsec to 500nsec, giving more time to Nordic to execute a Burst Cycle without retry. If PCIMGPU pull-up is hooked to MD[23], PCIPU is no longer needed, as both select PCI bus. This saves the need for two external pull-ups in PCI: only one external pull-up is needed to select PCI bus with reduced (MD16) or extended (MD23) Min-Gnt Value.

03/20/94 rev. 3.6 Modifications

1. For RAMDAC Layout related reasons, IREF, RED, GREEN and BLUE moved down three pins. FPVEE, FCBLANKn and TWRn moved up to fill the gap. No functional change.

Panel Interface Data Formats (compatible with 62xx family except 18/24 bit TFT)

<u>IFI</u> 24/ 18/ 12/ 9 bit	<u>Pin</u>	<u>STN Color</u> 16bit/8bit	<u>Monochrome</u> dual STN / single TFT
<u>Name</u>	<u>Pin</u>	<u>DB44#</u>	
R7/R5/R3/R2	140	(13) SUD3 / ---	---
R6/R4/R2/R1	139	(14) SUD2 / ---	---
RS/R3/R1/R0	138	(15) SUD1 / ---	---
R4/R2/R0	137	(16) SUD0 / ---	---
R3/R1	136	(9) SUD7 / ---	---
R2/R0	135	(10) SUD6 / ---	---
R1	134	---	---
R0	133	---	---
G7/G5/G3/G2	131	(8) SLD7 / sld3	UD3 / TD7
G6/G4/G2/G1	130	(7) SLD6 / sld2	UD2 / TD6
G5/G3/G1/G0	129	(6) SLD5 / sld1	UD1 / TD5
G4/G2/G0	128	(5) SLD4 / sld0	UD0 / TD4
G3/G1	127	(11) SUD5 / ---	---
G2/G0	126	(12) SUD4 / ---	---
G1	125	---	---
G0	123	---	---
B7/B5/B3/B2	122	(4) SLD3 / sld3	LD3 / TD3
B6/B4/B2/B1	120	(3) SLD2 / sld2	LD2 / TD2
B5/B3/B1/B0	119	(2) SLD1 / sld1	LD1 / TD1
B4/B2/B0	118	(1) SLD0 / sld0	LD0 / TD0
B3/B1	117	MOD	MOD
B2/B0	116	---	---
B1	115	(23) ---	---
B0	114	---	---
FPVDCLOCK	113	(18) SCLK / XCLKL	SCLK
LLCLK	112	(35) LP	LP
LFS	110	(22) FLM	FLM
FPDE	108	(26) --- / XCLKU	--- / DE

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